Alexandria University
Faculty of Engineering
Communications and Computers Department
Final Exam, Spring 2015

جامعة الإسكندرية
كلية الهندسة
قسم هندسة الإتصالات والحاسبات
امتحان نهاية الفصل الدراسي الثاني (ربيع ٢٠١٥)

Course Title and Code Number:
Digital Integrated Circuits Design (CC401)
Time Allowed: 2 Hours

اسم المقرر والرقم الكودي له: تصنيع و تصميم
تصميم الدوائر المتكاملة الرقميةً (CC401)
الزمن: ساعتين

Answer all questions: **(50 marks)**

Question 1: **(15 marks)**

Consider the AOI logic function:

$$y = \overline{a(b+c)(d+e+f)}$$

a) Design a CMOS circuit realizing this function using the fewest number of transistors.
b) Is it possible to find an equivalent nFET and pFET Euler paths for the circuit? If so, construct a colored stick diagram layout. If not, find a layout strategy and construct the corresponding stick diagram.
c) Determine the transistor sizes relative to a basic symmetric inverter of $(W/L)_n$ and $(W/L)_p$ size such that the logic circuit has approximately the same propagation delays as the inverter.
d) Draw the gate voltage transfer characteristics and indicate all important values on it.
e) Find the gate worst values of fall and rise time.

V_{DD}=5 V, $|V_{T0}|$=1 V, C_L=5pF
μp Cox = 20 μA/V2, μn Cox = 50 μA/V2, $(W/L)_n$ =0.5μm/0.25μm,

Question 2: **(12 marks)**

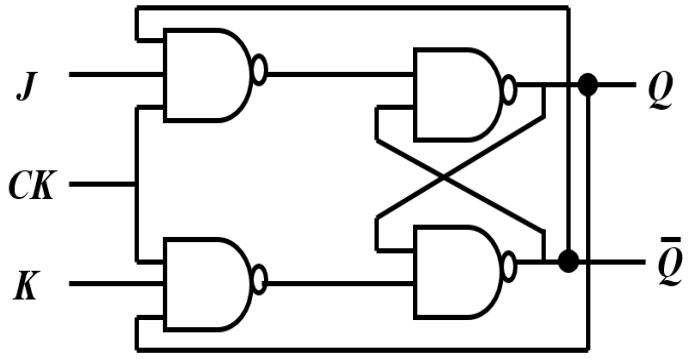
a) Design a circuit realizing this function using transmission gates with the fewest number of transistors.

$$y = ab + \bar{a}c + \bar{b}c$$

b) Design an 8-to-1 multiplexer using transmission gates.
c) Show how the multiplexer you developed in (b) can be used to realize the function of (a).
d) What are the advantages of transmission gates over pass transistor logic?

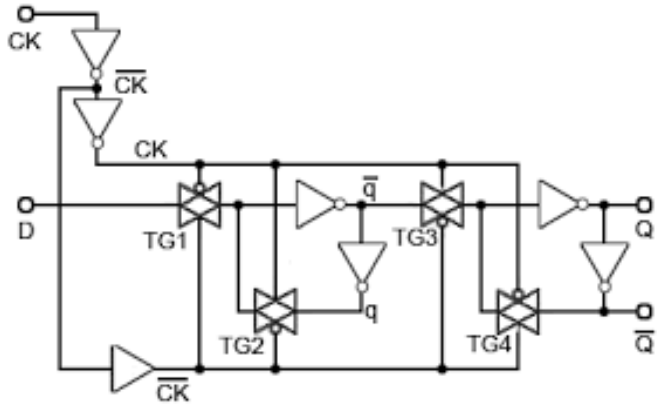
Question 3: **(9 marks)**

a) Design a CMOS Circuit realizing the following JK Latch using the fewest number of transistors.



b) Establish the truth table of the JK latch of part (a) indicating each mode of operation.

c) Identify the type of the following gate and briefly describe its operation with the input CK.



Question 4: **(14 marks)**

a) Design an active high 4x4 ROM having the following truth table.

Address	d_3	d_2	d_1	d_0
0	1	0	1	0
1	0	1	0	0
2	1	0	0	1
3	0	0	1	1

b) Design the column and row address decoders of the ROM circuit of part (a).

c) Calculate the total number of transistors used by the ROM circuit of part (a) and its decoders of part (b)

d) A single-transistor DRAM cell is represented by the following circuit diagram. The bit line can be pre-charged to VDD/2 by using a clocked pre-charge circuit. Also the WRITE circuit is assumed here to bring the potential of the bit line to VDD or 0 V during the WRITE operation with word line at VDD. Using the parameters given: $V_{T0} = 1\ V,\ \gamma = 0.3\ V^{1/2},\ |2\phi_f| = 0.6\ V$

Find the maximum voltage across the storage capacitor Cs after WRITE-1 operation, i.e., when the bit line is driven to VDD = 5 V. Assuming zero leakage current in the circuit, find the voltage at the bit line during READ- operation after the bit line is first pre-charged to VDD/2.