Question # 1.2

Calculate how many clock cycles will take execution of this segment on the simple pipeline without forwarding or bypassing when result of the branch instruction (new PC content) is available after WB stage. Show timing of one loop cycle in Figure 1.1:

Instruction	Clock cycle number																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LW R1, 0 (R4)																	
LW R2, 400 (R4)																	
ADDI R3,R1,R2																	
SW R3, 0 (R4)																	
SUB R4, R4, #4																	
BNEZ R4, L1																	

Figure 1.1

Solution

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
LW R1, 0 (R4)	IF	ID	Ex	M	W											
LW R2,400(R4)		IF	ID	Ex	M	W										
ADDI R3,R1,R2			IF	ID	*	*	Ex	M	W							
SW R3, 0 (R4)				IF	*	*	ID	Ex	*	M	W					
SUB R4, R4, #4							IF	ID	*	Ex	M	W				
BNEZ R4, L1								IF	*	ID	*	*	Ex	M	W	

Question # 1.3

Calculate how many clock cycles will take execution of this segment on the simple pipeline with normal forwarding and bypassing when result of branch instruction (new PC content) is available after completion of the ID stage. Show timing of one loop cycle in Figure 1.2.

Instruction	Clock cycle number																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LW R1, 0 (R4)																	
LW R2, 400 (R4)																	
ADDI R3,R1,R2																	
SW R3, 0 (R4)																	
SUB R4, R4, #4																	
BNEZ R4, L1																	

Figure 1.2

Solution

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
LW R1, 0 (R4)	IF	ID	Ex	M	W											
LW R2,400(R4)		IF	ID	Ex	M	W										
ADDI R3,R1,R2			IF	ID	*	Ex	M	W								
SW R3, 0 (R4)				IF	*	ID	Ex	M	W							
SUB R4, R4, #4						IF	ID	Ex	M	W						
BNEZ R4, L1							IF	ID	Ex	M	W					

1- How many register values need to be forwarded in the following code?
add R3, R4, R5
sub R2, R3, R4
beq R2, R3, done
a. 1
b. 2
c. 3
d. 4

c

2- What happens in the MEM stage for an addi instruction?
a. Nothing
b. Load the value
c. Calculate the ALU result
d. Write back the ALU result

a

3- What is the most important thing for getting performance from a pipelined design?
a. Have as few pipeline registers as possible
b. Make each stage fast
c. Keep the pipeline full
d. All of the above

c

4- What is needed to resolve the following hazard?
lw R4, 12(R14)
add R14, R4, R13
a. Forwarding from WB to EX
b. Forwarding from MEM to EX
c. Double-pumping the RF
d. Can’t resolve: need to stall

d

5- How many branch delay slots do we have if the branch decision is made in the MEM stage?
a. 0
b. 1
c. 2
d. 3

d

6- How many hazards does the code below have for the standard 5-stage MIPS pipeline without any forwarding logic?

```
Add r1, r2, r3
Add r4, r2, r2
Ld r5, 0(r4)
Add r4, r5, r4
```

a. 0
b. 1
c. 2
d. 3

d

Pipelining [12 points]

8a. Identify all data dependencies in the following code. [2 points]

Fill in the table below for each data dependency you find. For example, if instruction 2 depends on register 14 from instruction 0, you would write "R14 from 2". If there is no data dependency leave the table entry blank.

Instruction	Depends on Register from Instruction	Depends on Register from Instruction	Depends on Register from Instruction
I1: `add $r2, $r1, $r3`			
I2: `sub $r4, $r2, $r1`			
I3: `and $r5, $r1, $r2`			
I4: `sub $r6, $r2, $r4`			
I5: `add $r7, $r2, $r3`			

Assume a standard 5-stage MIPS pipeline discussed in class (IF, ID, EX, MEM, WB). Fill out the schedule for executing the above instructions correctly. The cycles (time) are on the horizontal axis. Fill in IF, ID, EX, MEM, and WB in the appropriate time for each instruction. Label all stalls with * and draw arrows on the scheduling to specify what is forwarded and where. The shading and lines are just to make it easier to grade and have nothing to do with the problem.

8b. Fill out the schedule for a pipeline with no forwarding. [5 points]

	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14
I1															
I2															
I3															
I4															
I5															

8b. Fill out the schedule for a pipeline with forwarding from just the EX/MEM stage. [5 points]

	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14
I1															
I2															
I3															
I4															
I5															

Pipelining [12 points]

8a. Identify all data dependencies in the following code. [2 points]

Fill in the table below for each data dependency you find. For example, if instruction 2 depends on register 14 from instruction 0, you would write "R14 from 2". If there is no data dependency leave the table entry blank.

Instruction	Depends on Register from Instruction	Depends on Register from Instruction	Depends on Register from Instruction
I1: `add $r2, $r1, $r3`			
I2: `sub $r4, $r2, $r1`	*R2 from 1*		
I3: `and $r5, $r1, $r2`	*R2 from 1*		
I4: `sub $r6, $r2, $r4`	*R2 from 1*	*R4 from 2*	
I5: `add $r7, $r2, $r3`	*R2 from 1*		

Assume a standard 5-stage MIPS pipeline discussed in class (IF, ID, EX, MEM, WB). Fill out the schedule for executing the above instructions correctly. The cycles (time) are on the horizontal axis. Fill in IF, ID, EX, MEM, and WB in the appropriate time for each instruction. Label all stalls with * and draw arrows on the scheduling to specify what is forwarded and where. The shading and lines are just to make it easier to grade and have nothing to do with the problem.

8b. Fill out the schedule for a pipeline with no forwarding. [5 points]

	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14
I1	*IF*	*ID*	*EX*	*MEM*	*WB*										
I2		*IF*	*ID*	*	*	*EX*	*MEM*	*WB*							
I3			*IF*	*ID*	*	*	*EX*	*MEM*	*WB*						
I4				*IF*	*ID*	*	*	*	*EX*	*MEM*	*WB*				
I5					*IF*	*ID*	*	*	*	*EX*	*MEM*	*WB*			

8b. Fill out the schedule for a pipeline with forwarding from just the EX/MEM stage. [5 points]

	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14
I1	*IF*	*ID*	*EX*	*MEM*	*WB*										
I2		*IF*	*ID*	*EX*	*MEM*	*WB*									
I3			*IF*	*ID*	*	*EX*	*MEM*	*WB*							
I4				*IF*	*ID*	*	*EX*	*MEM*	*WB*						
I5					*IF*	*ID*	*	*EX*	*MEM*	*WB*					

$r2 is forwarded from I1's MEM in T3 to I2's EX in T3.