1- Which data will be in a 4-entry, direct-mapped cache with one byte per line after the following memory accesses?
address: 0, 1, 2, 3, 4, 5, 3, 2, 1

a. 1, 2, 3, 4
b. 1, 2, 3, 5
c. 1, 3, 4, 5
d. 1, 2, 4, 5

2- Which data will be in a 4-entry, fully-associative, LRU cache with one word per line after the following memory accesses?
address: 0, 1, 2, 3, 4, 5, 3, 2, 1

a. 1, 2, 3, 4
b. 1, 2, 3, 5
c. 1, 3, 4, 5
d. 1, 2, 4, 5

3- How many hits will the following access pattern generate in a 2-way set associative cache with 8 entries. (Assume the line size is 1 entry per line.) 4, 5, 6, 12, 13, 4, 5, 1, 12, 13, 5
a. 2
b. 3
c. 4
d. 5

4. Assume you have a 2-way set-associative LRU cache with 4 entries and a cache line size of 1 bytes. What will the hit (H) miss (M) pattern be for the following access pattern: 0 1 2 3 7 0 3 8 1?
a. M M M M M M H M M
b. M M M M M H M M H
c. M M M M M H H M M
d. M M M M M H H M H

5- Which data will be in a 4-entry, direct-mapped cache with one byte per line after the following memory accesses?
Address: 0, 1, 2, 3, 4, 5, 3, 2, 1, 2, 5
a. 1, 2, 3, 4
b. 0, 2, 4, 5
c. 2, 3, 4, 5
d. 0, 1, 3, 4

6- Which data will be in a 4-entry, direct-mapped, cache with a least-recently-used replacement policy and one byte per line after the following memory accesses?
address: 3, 2, 1, 0, 4, 5, 3, 1, 2
a. 1, 2, 3, 5
b. 1, 2, 3, 4
c. 1, 3, 4, 5
d. 1, 2, 4, 5

7- Which data will be in a 4-entry, fully-associative, cache with a least-recently-used replacement policy and one byte per line after the following memory accesses?
address: 3, 2, 1, 0, 4, 5, 3, 1, 2
a. 1, 2, 3, 5
b. 1, 2, 3, 4
c. 1, 3, 4, 5
d. 1, 2, 4, 5

Caches [16 points]

6. Show the contents of the three caches below for the specified address stream. [9 points; 3 for each cache type]
Three, 4-entry, LRU caches are shown below, with the most recently used entry at the top of each set. They are fully-associative (FA), direct-mapped (DM), and 2-way set-associative (SA). Each cache has a block/line size of 1 byte/address. The DM and SA caches use the modulo (LSB-based) indexing function discussed in class. Show how the contents of the caches change with the access pattern 0, 1, 2, 3, 4, 0, 4, 0 ,2 by writing the memory address in each location of the cache at each time step and circling whether the access is a hit or miss.

Cycle 0: Address: 0

FA		DM		SA	
0 - MISS		*0 - MISS*		*0 - MISS*	
Hit	Miss	Hit	Miss	Hit	Miss

Cycle 1: Address: 1

FA		DM		SA	
1 - MISS		*0*		*0*	
0		*1 - MISS*			
				1 - MISS	
Hit	Miss	Hit	Miss	Hit	Miss

Cycle 2: Address: 2

FA		DM		SA	
2 - MISS		*0*		*2 - MISS*	
1		*1*		*0*	
0		*2 - MISS*		*1*	
Hit	Miss	Hit	Miss	Hit	Miss

Cycle 3: Address: 3

FA		DM		SA	
3 - MISS		*0*		*2*	
2		*1*		*0*	
1		*2*		*3 - MISS*	
0		*3 - MISS*		*1*	
Hit	Miss	Hit	Miss	Hit	Miss

Cycle 4: Address: 4

FA		DM		SA	
4 - MISS		*4 - MISS*		*4 - MISS*	
3		*1*		*2*	
2		*2*		*3*	
1		*3*		*1*	
Hit	Miss	Hit	Miss	Hit	Miss

Cycle 5: Address: 0

FA		DM		SA	
0 – MISS		*0 - MISS*		*0 - MISS*	
4		*1*		*4*	
3		*2*		*3*	
2		*3*		*1*	
Hit	Miss	Hit	Miss	Hit	Miss

Cycle 6: Address: 4

FA		DM		SA	
4 – HIT		*4 - MISS*		*4 – HIT*	
0		*1*		*0*	
3		*2*		*3*	
2		*3*		*1*	
Hit	Miss	Hit	Miss	Hit	Miss

Cycle 7: Address: 0

FA		DM		SA	
0 – HIT		*0 - MISS*		*0 – HIT*	
4		*1*		*4*	
3		*2*		*3*	
2		*3*		*1*	
Hit	Miss	Hit	Miss	Hit	Miss

Cycle 8: Address: 2

FA		DM		SA	
2 – HIT		*0*		*2 - MISS*	
0		*1*		*0*	
4		*2 – HIT*		*3*	
3		*3*		*1*	
Hit	Miss	Hit	Miss	Hit	Miss

(Extra)

FA		DM		SA	
Hit	Miss	Hit	Miss	Hit	Miss

Problem 3: Caches [23 points]

Three, 4-entry, LRU caches are shown below, with the most recently used entry at the top of each set. They are fully-associative (FA), direct-mapped (DM), and 2-way set-associative (SA). Each cache has a block/line size of 1 byte/address. The DM and SA caches use the modulo (LSB-based) indexing function discussed in class. Show how the contents of the caches change with the access patterns below by writing the memory address in each location of the cache after each access at each time step and circling whether the access is a hit (H) or miss (M).

A): 0, 8, 4, 8, 4, 0 [6 points]

Cycle 0—0

FA	DM	SA
0	0	0
M	M	M

Cycle 1—8

FA	DM	SA
8	8	8
0		0
M	M	M

Cycle 2—4

FA	DM	SA
4	4	4
8		8
0		
M	M	M

Cycle 3—8

FA	DM	SA
8	8	8
4		4
0		
H	M	H

Cycle 4—4

FA	DM	SA
4	4	4
8		8
0		
H	M	H

Cycle 5—0

FA	DM	SA
0	0	0
4		4
8		
H	M	M

B) Hit ratios: (ratio of hits to total accesses) [5 points]

FA: 50 % DM: 0 % SA: 33 %

Briefly explain the differences (or lack thereof) in miss ratios:

DM: all accesses map to the same line so they always miss; SA is more flexible because it can hold two conflicting addresses; FA can hold all of them.

C): 0, 1, 2, 1, 2, 0 [6 points]

Cycle 0—0

FA	DM	SA
0	0	0
M	M	M

Cycle 1—1

FA	DM	SA
1	0	0
0	1	
		1
M	M	M

Cycle 2—2

FA	DM	SA
2	0	2
1	1	0
0	2	1
M	M	M

Cycle 3—1

FA	DM	SA
1	0	2
2	1	0
0	2	1
H	H	H

Cycle 4—2

FA	DM	SA
2	0	2
1	1	0
0	2	1
H	H	H

Cycle 5—0

FA	DM	SA
0	0	0
2	1	2
1	2	1
H	H	H

D) Hit ratios: (ratio of hits to total accesses) [5 points]

FA: 50 % DM: 50 % SA: 50 %

Briefly explain the differences (or lack thereof) in miss ratios:

The addresses map nicely for all three caches so they behave the same.

E) Explain why B and D show (or do not show) different hit ratios for the caches: [1 point]

The address streams are different so the caches behave differently.