AAST
Faculty of Engineering
CE-Department
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Fifth Term
EC233: Devices II
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Sheet : 3

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1. Given an n-channel enhancement-type MOSFET made of silicon with source connected to substrate:

$$\epsilon_{ox} = 3.9.$$
$$\overline{\mu} = 600\ cm^2/V.sec.$$
$$l = 2.5*10^{-4}\ cm.$$
$$t_{ox} = 8*10^{-6}\ cm.$$
$$Z = 1.8*10^{-3}\ cm.$$
$$V_t = 1.5\ V,$$

and substrate acceptor concentration $N_a = 10^{16}\ cm^{-3}$

   a) Compute gate oxide capacitance.
   b) Compute I_{Dsat} (saturation drain current) for values of V_{GS} ranging from 0 to 5 V in 1 volt intervals.
   c) Determine the the linear conductance of this device near $V_{DS} = 0$ for $V_{GS} =$ 2, 3, 4 and 5 V.

2. For the device above:

   a) Find g_m for $V_{GS} = 2, 3, 4$ and 5 V.
   b) Repeat (a) if the channel length is reduced by a factor of 2.

3. Assume that the drain space charge width of the MOSFET of problem (1) increases by 0.1 μm/V of drain-source voltage.

   a) Calculate the active region output conductance g_{os} for gate voltages of 2 and 5 V.
   b) Repeat (a) if the channel is reduced in length by 2.

4. Determine approximately the maximum drain voltage capability of the device of problem (1) if this is limited by reach-through of the drain space charge region to the source space charge region. How is the value affected if the channel width is halved? How is this affected by the substrate doping?