Alexandria University
Faculty of Engineering
EE-Department

EE-Communications | **Year: 2^{nd}**
Logic Design | **Sheet 1**
Instructor: Dr. M. El-Banna | **EE242**

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1. Obtain the circuit for the following functions using only NAND gates:
   a. $f(A,B,C,D) = \sum_m(1,4,10,11,13,15)$
   b. $f(A,B,C,D) = \sum_m(1,3,4,9,10,13)$
   c. $f(A,B,C,D) = \sum_m(1,8\text{-}10,15)$
   d. $f(A,B,C,D,E) = \sum_m(1,3\text{-}7,11,14\text{-}17,22,24\text{-}27,30)$
   e. $f(A,B,C,D,E) = \sum_m(1,8\text{-}10,13\text{-}17,21,25\text{-}27,30,31)$

2. Obtain NOR circuits for the functions of Problem 1.

3. a. Use a single level of 1-of-8 MUXs and a few assorted gates (if needed) to obtain a combinational circuit for each of the functions of Problem 1.

   b. For each of your solutions, complement one variable and rearrange the inputs so that the function is still correct.

4. Using 1-of-4 MUXs, obtain a two-level MUX circuit for each of the functions of problem 1.

5. Obtain the circuit for the function $f(A,B,C,D,E) = \sum_m(0,1,6,7,9,12,13,15,18,20,22,24\text{-}26,28)$ using two levels of 1-of-4 MUXs and a few assorted gates.

6. Implement the following functions using ROMs and PLAs:

   a. $f(A,B,C,D) = \sum_m(1,2,5,7,8,10,13,14)$
   b. $f(A,B,C,D) = \sum_m(2,3,6,7,9,11,12,13)$
   c. $f(A,B,C,D) = \sum_m(0,2,3,6\text{-}8,10,13)$
   d. $f(A,B,C,D) = \sum_m(0,6,9,10,15)$

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Logic Design | **Sheet 2**
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1. Design an FA circuit using logic gates suitable for adding two bits of addend,two bits of augend, and carry-in input.
2. Obtain a single-bit FA using only MUXs.
3. Design a single-bit FA using only NOR gates.
4. Use the FAs designed in Problem 1 to perform addition of six-bit numbers. Show the configuration of the setup for adding $(110110)_2$ and $(000010)_2$.
5. Design a four-bit FA using combinatinal logic.
6. Design a four-bit FA using ROM technology.

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EE-Communications — **Year: 2nd**
Logic Design — **Sheet 3**
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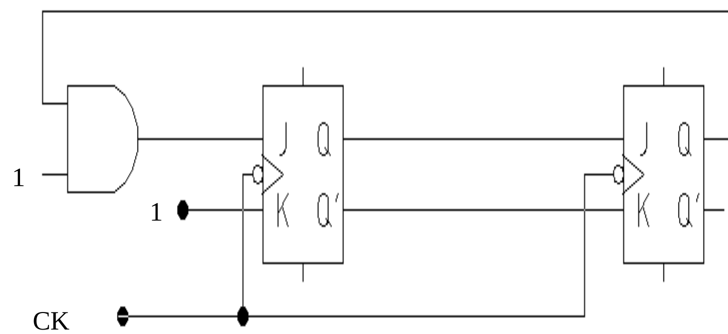
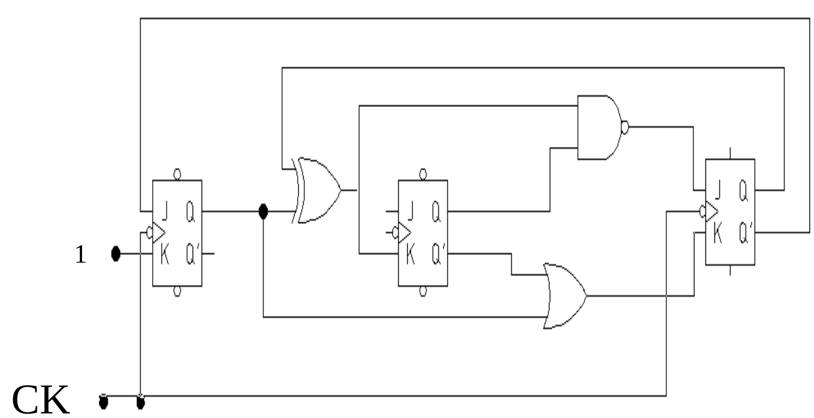
1. Draw the timing diagram for the given input signal and circuit of figure below. Assume the starting value of $Q_2Q_1 = 0$

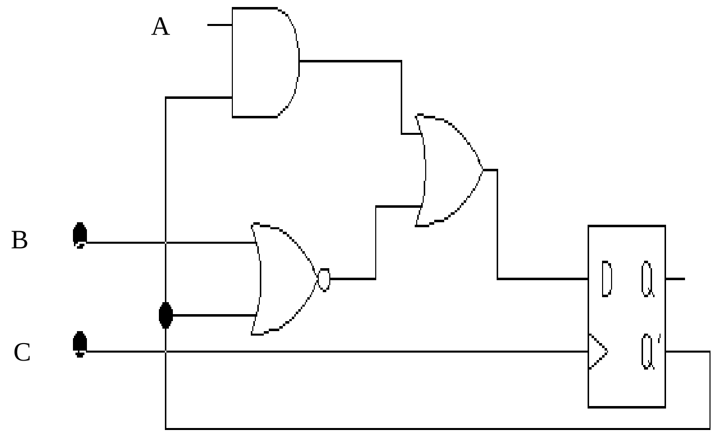


2. What sequence should repeat for the sequential circuit of figure below for the following initial inputs:
   a. $Q_3Q_2Q_1 = 001$ b. $Q_3Q_2Q_1 = 100$



3. Obtain a TTF from a DFF.

4. Explain the behavior of the circuit of Figure below.


A
B
C
D
Q
Q'

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EE-Communications	**Year: 2nd**
Logic Design	**Sheet 4**
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1. Design a three-bit that counts up when a control variable E=0, and counts down when E=1

2. Design a four-bit binary up-counter using JK FFs.

3. Design a synchronous sequential circuitusing SR FFs that result in an output of 1 whenever each of the following sequences occurs:
   a. 0001 e. 10010
   b. 0101 f. 11011
   c. 1101 g. 10011
   d. 1011 h. 11011

4. Repeat Problem 3 using JK FFs.

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Logic Design | **Sheet 5**
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1. Repeat Problem 3 sheet (3) using T FFs.

2. Assume a two-bit binary counter that counts up when A=1 and B=0; counts down when A=0 and B=1; halts when A=0 and B=0;and is forbidden to operate when A=B=1. Obtain the state diagram and the JK eqations.

3. Obtain the equivalent Mealy sate table from the machine of the figure below.

PS	NS		z
	X=0	X=1	
A	A	C	0
C	D	C	0
D	D	E	1
E	A	E	0