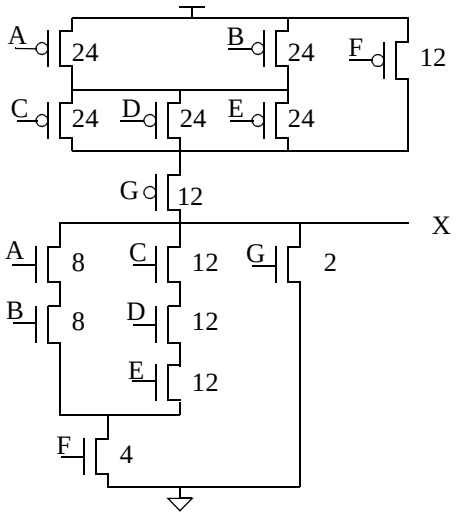
# Chapter 6
# PROBLEMS

**1.** [E, None, 4.2] Implement the equation $X = ((\overline{A} + \overline{B})\,(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\,\overline{G}$ using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 2$ and PMOS $W/L = 6$. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?

**Solution**

Rewriting the output expression in the form $X = ((\overline{A} + \overline{B})\,(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\,\overline{G} = \overline{((AB + CDE)F) + G}$ allows us to build the pulldown network by inspection (parallel devices implement an OR, and series devices implement an AND). The pullup network is the dual of the pulldown network.




The plot shows sizes that meet the requirement - in the worst case, the output resistance of the circuit matches the output resistance of an inverter with NMOS W/L=2 and PMOS W/L=6.

The worst case pull-up resistance occurs whenever a single path exists from the output node to Vdd. Examples of vectors for the worst case are ABCDEFG=1111100 and 0101110. The best case pull-up resistance occurs when ABCDEFG=0000000.

The worst case pull-down resistance occurs whenever a single path exists from the output node to GND. Examples of vectors for the worst case are ABCDEFG=0000001 and 0011110.

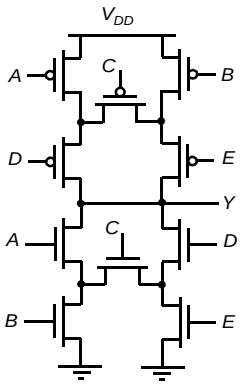
The best case pull-down resistance occurs when ABCDEFG=1111111.

**2.** Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors:

$$\overline{Y} = (A \cdot B) + (A \cdot C \cdot E) + (D \cdot E) + (D \cdot C \cdot B)$$

**Solution**

The circuit is given in the next figure.




**3.** Consider the circuit of Figure 6.1.

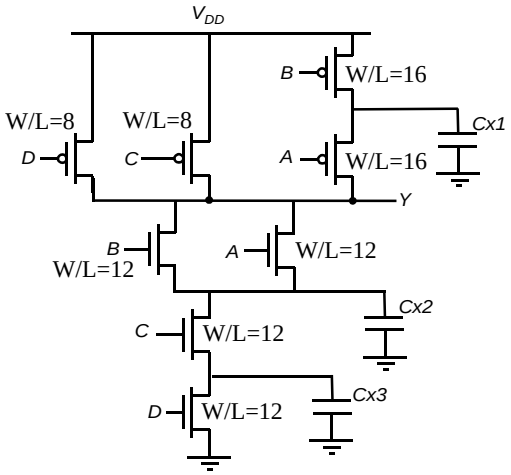



**Figure 6.1** CMOS combinational logic gate.

**a.** What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 4$ and PMOS $W/L = 8$.

**Solution**

The logic function is $: Y = \overline{(A + B)CD}$. The transistor sizes are given in the figure above.

**b.** What are the input patterns that give the worst case $t_{pHL}$ and $t_{pLH}$. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

**Solution**

The worst case $t_{pHL}$ happens when the internal node capacitances (*Cx2* and *Cx3*) are charged before the high to low transition. The initial states that can cause this are: ABCD=[1010, 1110, 0110]. The final state is one of: ABCD=[1011, 0111].

The worst case $t_{pLH}$ happens when *Cx1* is charged before the low to high transition. The input pattern that can cause this is: ABCD=[0111] =>[0011].

**c.** Verify part (b) with SPICE. Assume all transistors have minimum gate length (0.25μm).

**Solution**

The two cases are shown below.

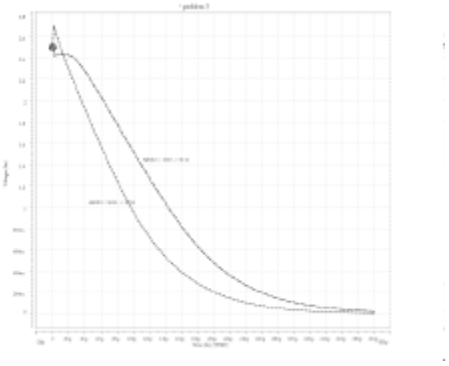


**Figure 6.2** Best and worst $t_{pHL}$.

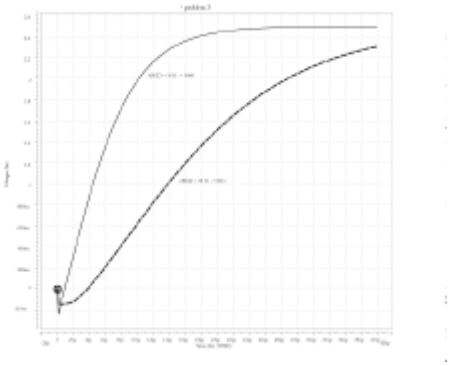


**Figure 6.3** Best and worst $t_{pLH}$.

**d.** If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume $V_{DD}$=2.5V, $C_{out}$=30fF and $f_{clk}$=250MHz.

**Solution**

Since D is always 1, the circuit implements the following function $Y = \overline{(A + B)C}$ .

$P_{(A+B)=1} = P_{A=0}.P_B = 0 = 0.5*(1-0.2) = 0.4$,

$P_{(A+B)=0} = 1 - 0.4 = 0.6$,

$P_{Y=0} = P_{(A+B)=1}.P_C = 1 = 0.6*0.3 = 0.18$

$P_{Y=1} = 1 - 0.18 = 0.82$

$P_{Y=0=>1} = 0.18*0.82 = 0.1476$

So $Pdyn = P_{Y=0=>1} C_{out} V_{DD}^2 f_{clk} = (0.1476)(30.10^{-15})(2.5^2)(250.10^6) = 6.92\,\mu W$.

**4.** [M, None, 4.2] CMOS Logic

**a.** Do the following two circuits (Figure 6.4) implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

**Solution**

Yes, they implement the same logic function :

$F = (\overline{ABCD + E}) = (\overline{A} + \overline{B} + \overline{C} + \overline{D}).\overline{E}$

**b.** Will these two circuits' output resistances always be equal to each other?

**Solution**

No

**c.** Will these two circuits' rise and fall times always be equal to each other? Why or why not?

**Solution**

No. Circuit B appears optimized for the case where the transistor with input E is on the critical path since it is closer to the output node than in circuit A. Therefore, if input E arrives later, circuit B will be faster than circuit A since the internal node will already be charged and only the output capacitance needs to be switched. Even if we assume, all inputs arrive at the same time, however, the two circuits rise and fall times will not be equal to each other. Consider an input combination where E,A,B,C,D are all low. Circuit A has only one body-affected device while circuit B has four. Since the associated rise in $V_t$ and fall in output resistance affects only one resistor in circuit A, but four parallel resistors in circuit B, we expect a difference in the timing waveforms.

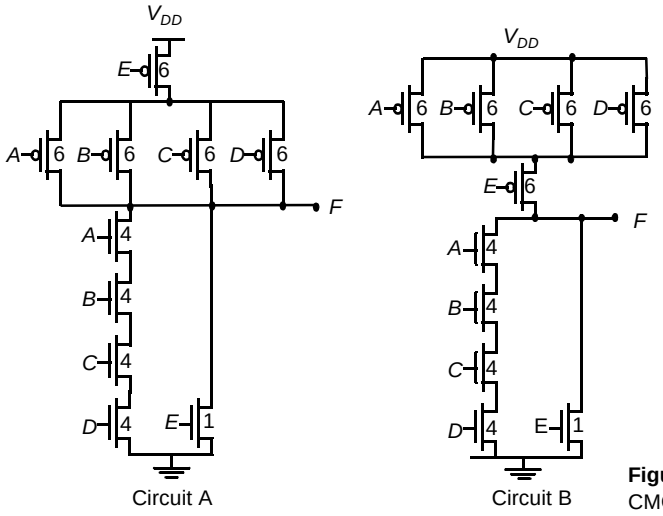



**Figure 6.4** Two static CMOS gates.

**5.** [E, None, 4.2] The transistors in the circuits of the preceding problem have been sized to give an output resistance of 13 kΩ for the worst-case input pattern. This output resistance can vary, however, if other patterns are applied.

**a.** What input patterns (*A*–*E*) give the lowest output resistance when the output is low? What is the value of that resistance?

**Solution**

The lowest output resistance is obtained when all inputs (A, B, C, D and E) are equal to 1. In that case, the output resistance is the parallel of the resistance of a nMOS of width 1, with a series of four equal nMOS of width 4. Both combinations have the same resistance, equal to the worst-case output resistance, 13 $k\Omega$ . Then the output resistance, in this case, is half this value, 6.5 $k\Omega$ .

**b.** What input patterns (*A*–*E*) give the lowest output resistance when the output is high? What is the value of that resistance?