## Alexandria Institute of Technology Electronics Section

Course: Digital Integrated Circuits Instructor: Prof. M. El-Banna



Sheet: 1 SAT and SUN

1. The data sheet of SN7400 quad 2-input NAND gate of the TIL family provides the following:

Logic-1 input voltage required at both input terminals to ensure a logic-0 level at the output : MIN (minimum) 2V.

Logic-0 input voltage required at either input terminal to ensure a logic-1 at the output : MAX (maximum) 0.8V.

Logic-1 output voltage: MIN 2.4 V, TYP (typical) 3.3 V

Logic-0 output voltage: TYP 0.22V, MAX O.4V.

Logic-0 level supply current: TYP 12mA, MAX 22mA (for the entire package).

Logic-1- level supply current: TYP 4mA, MAX 8Ma (for the entire package). Propagation delay time to logic-0 level: TYP 7 ns, MAX 15ns.

Propagation delay time to logic-1 level: TYP 11ns, MAX 22ns.

- a. Find the noise margin in both the 0 and the 1 states
- b. Assuming that the gate is in the 1 state 50% of the time and in the 0 state 50% of the time, find the average static power dissipated in a typical gate. The power supply voltage is 5V.
- c. Assuming that the gate drives a capacitance  $C_L = 45~pF$  and is switched at a 1 MHz rate, find the dynamic power dissipation per gate using the typical values of the logic 1 and 0 levels at the output.
- d. Find the typical value of the gate delay –power product ( neglect the dynamic power dissipation)
- 2. A logic inverter having negligible static power dissipation is switched at the rate of 1 MHz. If the inverter is operated from a 10V-power supply and drives a 50-pF capacitance, find the dynamic power dissipation and the average current drawn from the power supply. Assume that the output levels are close to 0 and 10 V.
- 3. Consider the basic inverter discussed in the lecture under the conditions that  $V^+=5.5V$ ,  $R_L=10k\Omega$  and the switch on resistance is  $1~k\Omega$ . Let  $V_{\it off}=0V$ . Find the values of  $V_{\it OL}$  and  $V_{\it OH}$ .
- 4. Let the inverter specified in 3 be fed with an ideal pulse having zero rise and fall times. Assuming that the switch operates instantaneously, find the propagation delays  $t_{PHL}$  and  $t_{PLH}$  and  $\tau_n$  that result with a 50-pF load capacitance.